

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: BYEONG RYEOL LEE

Application No.: Confirmation
No:
Filed: December 30, 2003 Group No.:
Examiner
For: METHOD OF FORMING ISOLATION STRUCTURES IN EMBEDDED
SEMICONDUCTOR DEVICE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPLICATION DATA SHEET
37 C.F.R. § 1.76

BIBLIOGRAPHIC DATA

1. Applicant information

First applicant: BYEONG RYEOL LEE
Citizenship: Republic of Korea
Residence: Seoul, Korea

2. Correspondence information

Correspondence for this application should be addressed as follows:

Customer No.: 00909

3. Application information

Title of Invention: METHOD OF FORMING ISOLATION STRUCTURES IN EMBEDDED SEMICONDUCTOR DEVICE

Docket number assigned to this application: 040008-0307457

Suggested Classification: Class:
Subclass:
Technology Center to which subject matter is assigned:

Total number of drawing sheets: 4

Type of application: Utility

Application is to be published. Suggested drawing figure for publication:

Secrecy order under § 5.2:

This application does not disclose subject matter of an application which is under a secrecy order pursuant to § 5.2.

4. Representative information

The following have a power of attorney or authorization of agent in this application:

Customer No.: 00909

5. Foreign priority information

Foreign priority is claimed for this application as follows:

Country: Republic of Korea
Application No.: 10-2002-0087273
Filing Date: December 30, 2002
Status: Pending

6. Assignee information

The assignee(s) of this application is/are:

Dongbu Electronics Co. Ltd.
891-10 Daechi-dong, Gangnam-gu
Seoul, 135-523
Korea
Extent of interest of assignee in application: 100%

Date: December 30, 2003

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